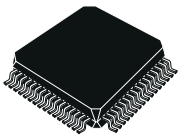
STM7E1

7 e 1 channels switch array

Features

- Main switches max. R_{ON} less than 2 Ω
- Provides 7 auxiliary switches with R_{ON} < 75 Ω
- 6 V_{PP} amplitude of analog input signal
- Digital inputs are TTL levels compatible



TQFP64

Description

The STM7E1A consists of 7 identical ISDN E1 channels, each channel corresponding to 4 main low-resistant switches (a and b) and 2 auxiliary switches (c and d). The switches positions in all the channels are identical and controlled by a unique control resource driven by the digital inputs Lm, Ls and Sc.

In each channel, the TX and RX lines can be switched between a Main port or a Spare-port by the main switches: if both "a" switches are closed and both "b" switches are open, the Main port is connected to the line, while if both "a" switches are open and both "b' switches are closed, the spare port is connected to the line.

The 2 auxiliary switches enable to close a local loop between the TX and RX access of a port: if "c" is closed, the Spare port RX and TX access is connected between each other to form a local loop, while if "d" is closed, the Main port RX and TX access is connected between each other to form a local loop.

The Spare port is only used for test purpose on the system board while the Main port is the communication channel. Consequently, a switching from the Main port to the Spare port occurs very rarely (<10 times a day).

The power supplies of the chip need to be de coupled properly. This means that at least one external capacitor C1 must be connected in between GND and VPOS, one external capacitor C2 between GND and VNEG, and one external capacitor C3 between each pair of VNEG and VPOS.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
STM7E1AR	-40 to 85 °C	TQFP64 (tape and reel)	1000 parts per reel

Contents

1 Application circuit

Figure 1. Typical operating circuit

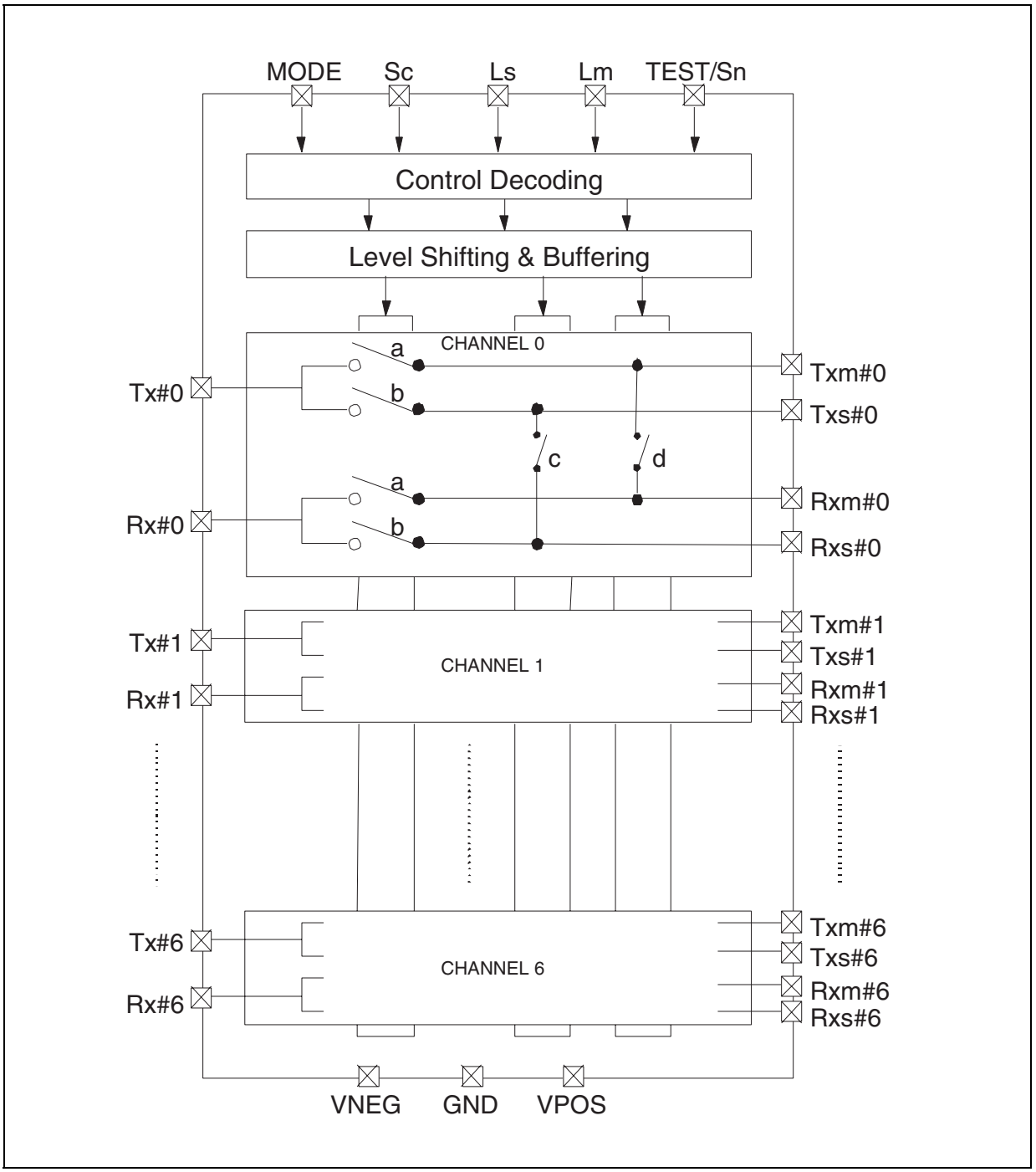


Table 2. Decoding of functional Mode 1 (Mode = L)

Switches	Status		Description
Main	Sc low	a closed, b open	Main port is connected to the line
	Sc high	a open, b closed	Spare port is connected to the line
Auxiliary	Lm low	d open	Main port local loop open
	Lm high	d closed	Main port local loop closed
	Ls low	c open	Spare port local loop open
	Ls high	c closed	Spare port local loop closed

When closing the main port local loop (Lm high), it is external system responsibility to ensure that the main port has previously been disconnected from the line (Sc has to be high). There is no internal mechanism to ensure this.

When closing the spare port local loop (Ls high), it is external system responsibility to ensure that the spare port has previously been disconnected from the line (Sc has to be high). There is no internal mechanism to ensure this.

Table 3. Decoding of functional Mode 2 (Mode = H)

Input	Outputs	
TEST/Sn	A_TX	B_TX
L	O	C
H	C	O

C = Closed

O = Open

Table 4. Decoding of functional Mode 2 (Mode = H)

Inputs			Outputs			
Sc	Lm	Ls	A_RX	B_RX	c	d
L	L	L	C	C	O	O
L	L	H	C	O	C	O
L	H	L	O	C	O	C
L	H	H	C	O	O	O
H	L	L	O	C	O	O

C = Closed

O = Open

1.1 Test mode description (mode = 0, test = 1)

In order to test the main switches (4-point measurement), test modes are foreseen where the main switches can be controlled independently from each other. One can enter in test mode by controlling the Sc, Lm and Ls pins according to the following table.

The digital part and auxiliary switches can be tested in functional mode

Table 5. Test mode

Signification	Sc	Lm	Ls
A_TX closed	H	H	L
A_RX closed	L	H	L
B_TX closed	H	L	H
B_RX closed	L	L	H
B_TX & c closed	H	L	L
A_RX & d closed	L	L	L
All main switches open	H	H	H
	L	H	H

Note: Although there is an internal pull down in the TEST pin, an external hardware connection from TEST to GND is required on the board to work in functional, mode.

2 Pin configuration

Figure 2. Pin configuration

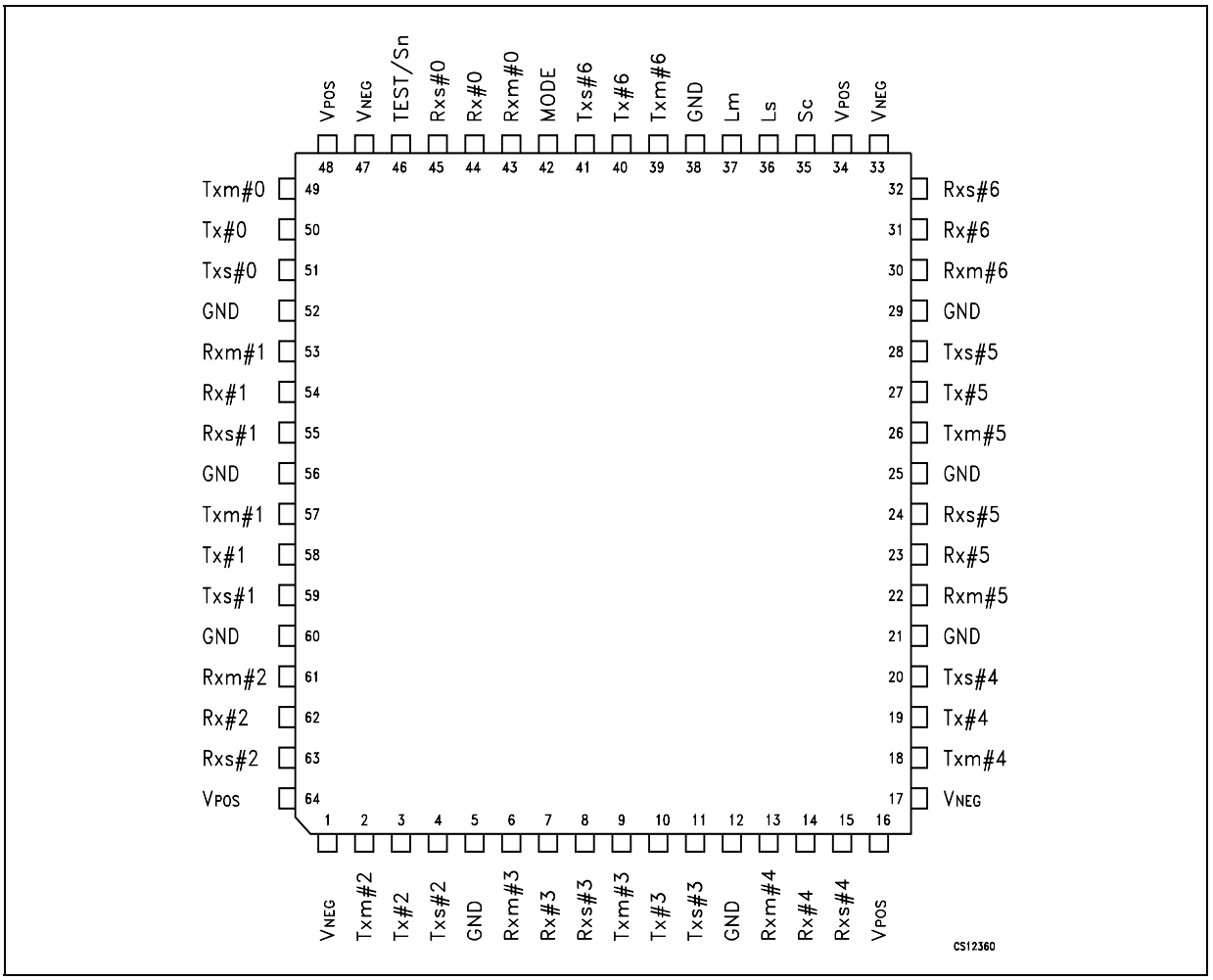


Table 6. Pin description

Pin n°	Symbol	Type	Name and function
1, 17, 33, 47	V_{NEG}(1)	P	Negative power supply
2	Txm#2	IOA	Channel 2: TX main port
3	Tx#2	IOA	Channel 2: TX line
4	Txs#2	IOA	Channel 2: TX spare port
5, 12, 21, 25, 29, 38, 52, 56, 60	GND	G	Voltage reference for digital inputs
6	Rxm#3	IOA	Channel 3: RX main port
7	Rx#3	IOA	Channel 3: RX line
8	Rxs#3	IOA	Channel 3: RX spare port
9	Txm#3	IOA	Channel 3: TX main port

Table 6. Pin description (continued)

Pin n°	Symbol	Type	Name and function
10	Tx#3	IOA	Channel 3: TX line
11	Txs#3	IOA	Channel 3: TX spare port
13	Rxm#4	IOA	Channel 4: RX main port
14	Rx#4	IOA	Channel 4: RX line
15	Rxs#4	IOA	Channel 4: RX spare port
16, 34, 48, 64	V_{POS}(2)	P	Positive power supply
18	Txm#4	IOA	Channel 4: TX main port
19	Tx#4	IOA	Channel 4: TX line
20	Txs#4	IOA	Channel 4: TX spare port
22	Rxm#5	IOA	Channel 5: RX main port
23	Rx#5	IOA	Channel 5: RX line
24	Rxs#5	IOA	Channel 5: RX spare port
26	Txm#5	IOA	Channel 5: TX main port
27	Tx#5	IOA	Channel 5: TX line
28	Txs#5	IOA	Channel 5: TX spare port
30	Rxm#6	IOA	Channel 6: RX main port
31	Rx#6	IOA	Channel 6: RX line
32	Rxs#6	IOA	Channel 6: RX spare port
35	Sc	I	Control digital input
36	Ls	I	Control digital input
37	Lm	I	Control digital input
39	Txm#6	IOA	Channel 6: TX main port
40	Tx#6	IOA	Channel 6: TX line
41	Txs#6	IOA	Channel 6: TX spare port
42	Mode	I	Control Digital Input
43	Rxm#0	IOA	Channel 0: RX main port
44	Rx#0	IOA	Channel 0: RX line
45	Rxs#0	IOA	Channel 0: RX spare port
46	TEST/Sn	I	Channel 6: RX main port
49	Txm#0	IOA	Channel 0: TX main port
50	Tx#0	IOA	Channel 0: TX line
51	Txs#0	IOA	Channel 0: TX spare port
53	Rxm#1	IOA	Channel 1: RX main port
54	Rx#1	IOA	Channel 1: RX line
55	Rxs#1	IOA	Channel 1: RX spare port
57	Txm#1	IOA	Channel 1: TX main port

Table 6. Pin description (continued)

Pin n°	Symbol	Type	Name and function
58	Tx#1	IOA	Channel 1: TX line
59	Txs#1	IOA	Channel 1: TX spare port
61	Rxm#2	IOA	Channel 2: RX main port
62	Rx#2	IOA	Channel 2: RX line
63	Rxs#2	IOA	Channel 2: RX spare port

Note: 1 All VNEG pins to be connected together on board.

2 All VPOS pins to be connected together on board.

3 Maximum ratings

Table 7. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
V_{POS}	Positive power supply voltage	V_{NEG} - 0.3	V_{NEG} + 7	V
GND	Reference ground	V_{NEG} - 0.3	V_{NEG} + 7	V
V_{IN}	Input voltage for digital inputs and analog input/output pins	V_{NEG} - 0.3	V_{NEG} + 7	V

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 8. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{POS}	Positive power supply voltage	3.3 - 5%		3.3 + 5%	V
V_{NEG}	Negative power supply voltage	-3.3 - 5%		-3.3 + 5%	V
T_{amb}	Ambient temperature	-25		85	°C
T_J	Junction temperature	-25		120	°C
$I_{peak, switch}$	Admissible peak current in 1 switch			300	mA
C_{la}	Load capacitance on ASIC output			70	pF

Table 9. Digital part specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{IL}	Low input level	0		0.8	V
V_{IH}	HigH input level	2		V_{POS}	V
V_{IT}	Low-high switching threshold voltage		1.6		V
I_{leak}	Input leakage current	-3		3	A

Table 10. Analog part specifications

Symbol	Parameter	Test condition	Value			Unit
			Min.	Typ.	Max.	
$R_{ON(main)}$(1)	On-resistance of the main switches			1.6	2	Ω
$R_{ON(aux)}$(1)	On-resistance of the auxiliary switches			50	75	Ω
$\Delta R_{ON(main)}$(1)	Difference of R_{ON} between devices	V_{IN} = 2V, T_A = 25°C		0.5		Ω
$\Delta R_{ON(main)}$(1)	Difference of R_{ON} between switches of the same device	V_{IN} = 2V, T_A = 25°C			0.8	Ω
R_{OFF}(1,2)	Off-resistance of the main and auxiliary switches		100			kΩ
C_{ON}(3)	Capacitance at any switch pin, switch ON			120		pF
C_{OFF}(3)	Capacitance at any switch pin, switch OFF			40		pF
$A_{peak,signal}$(1)	Peak amplitude of the signal at switch pins		-3		3	V_p
f_{signal}(1,4)	Frequency of the signal at switch pins (3dB bandwidth)		50		12000	kHz
Cross-talk(1,5)	Cross-talk between lines			4	8	mV_{rms}
t	Switch time of the main switches (a and b)			0.15	1	µs

Note: 1 All the parameters are valid only with a 75Ω (5%) load to GND.

2 Measured with a 5 V DC voltage applied to a closed switch.

3 Not tested in production.

4 Measured with a 2 V_{PP} signal.

5 Measured with the line connected to GND at one side with a 75 Ωresistor and all the other lines driven by a 1 MHz, 2 V_{PP} sine wave signal.

6 During the switching between the main and spare ports, the behavior of the component is not guaranteed: both main switches can be open (break before make).

7 Measured with the line switching from a 2.5 V DC level (main or spare port) to a -2.5 V DC level (spare or main port).

Table 11. Current consumption specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
P_{main}(1)	Maximal average power dissipation in the main switches			40	mW
P_{aux}(1)	Maximal average power dissipation in the auxiliary switches			150	mW
$I_{STDBY(VNEG)}$(1,3)	Standby (no switching) current of VNEG	-500		500	µA
$I_{STDBY(VPOS)}$(1,3)	Standby (no switching) current of VPOS	-500		500	µA
$E_{SWITCH(VNEG)}$(1)	Energy to be delivered to by VPOS when switching	-100		100	nJ
$E_{SWITCH(VPOS)}$(1)	Energy to be delivered to by VPOS when switching	-100		100	nJ

Note: 1 These parameters are not tested in production.

2 This power is not delivered by V_{POS} and V_{NEG} supplies but by the signal sources.

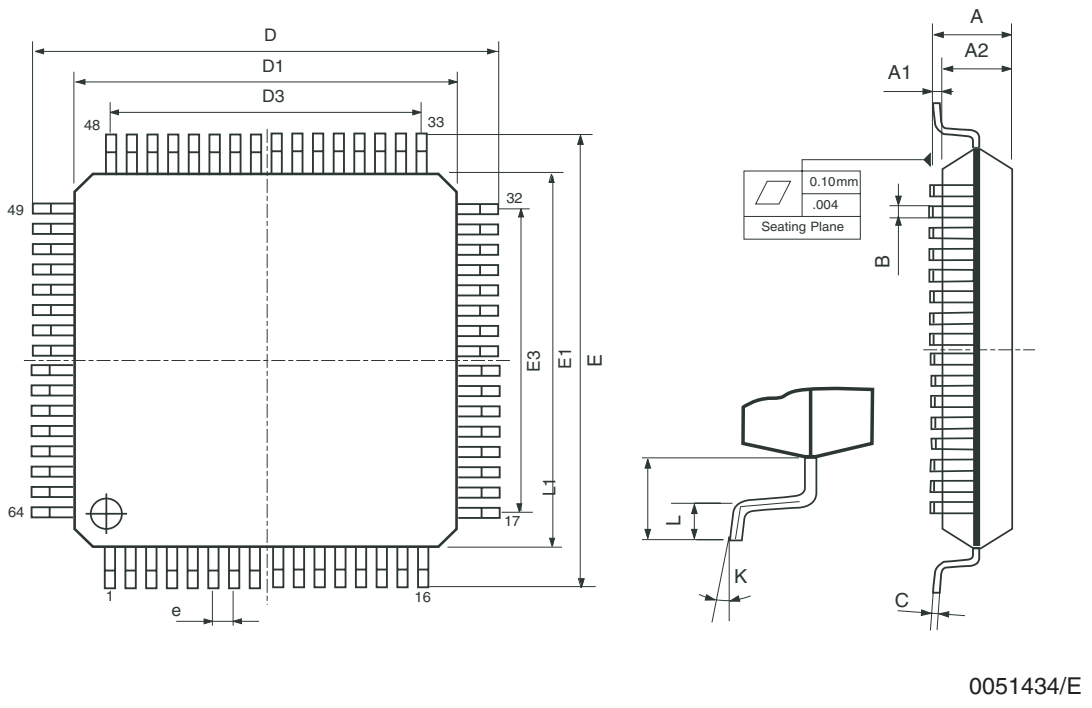
3 Only valid with digital inputs to GND or V_{POS} levels.

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TQFP64 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.6			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.465	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.402
D3		7.50			0.295	
E	11.80	12.00	12.20	0.465	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.402
E3		7.50			0.295	
e		0.50			0.020	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°	3.5°	7°	0°	3.5°	7°



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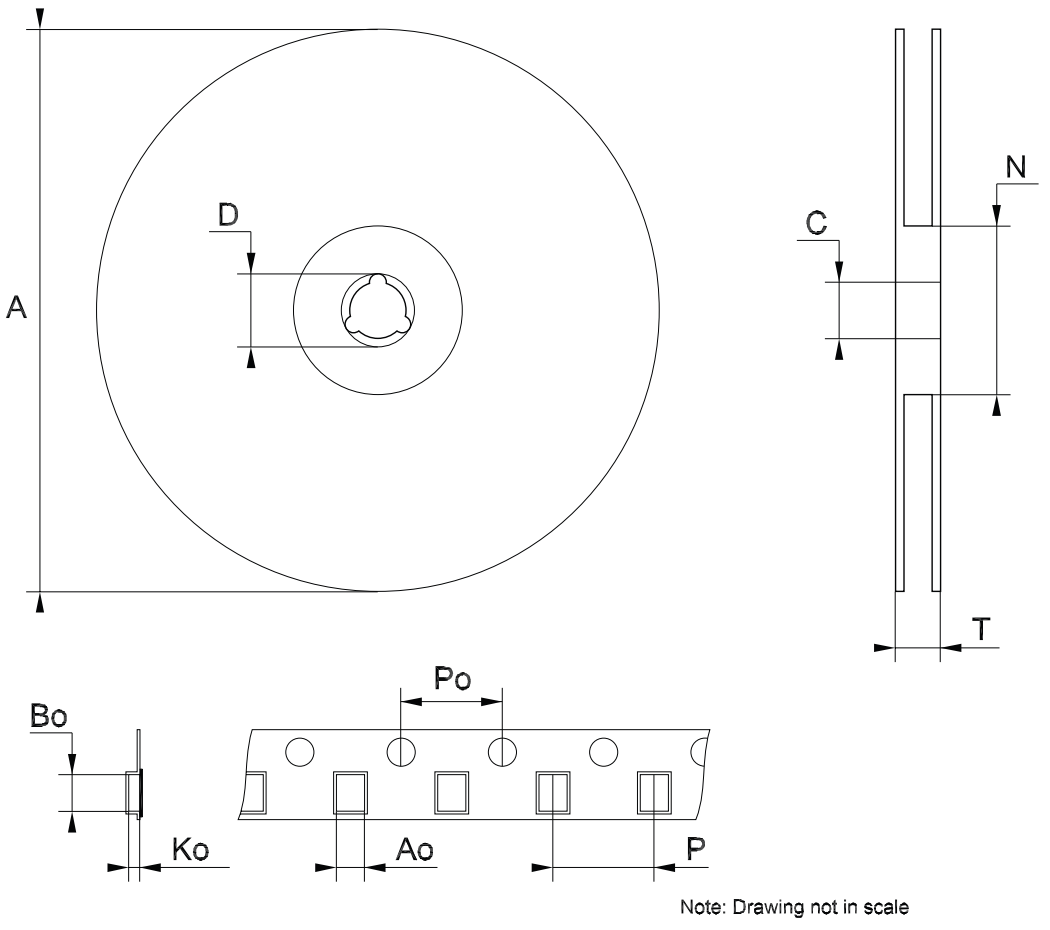
Tape & reel TQFP64 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.196
Ao	12.25		12.45	0482		0.490
Bo	12.25		12.45	0482		0.490
Ko	2.1		2.3	0.083		0.091
Po	3.9		4.1	0.153		0.161
P	15.9		16.1	0.626		0.639



Note: Drawing not in scale

5 Revision history

Table 12. Document revision history

Date	Revision	Changes
22-Jun-2004	2	
15-Nov-2007	3	Added *Table 1.*

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